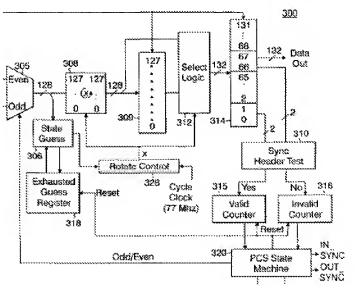
REMARKS/ARGUMENTS

Claims 1 and 13 are amended and new claims 21-25 are added in this application. Claims 1-9 and 18-20 were previously canceled. Accordingly, claims 10-17 and 21-25 remain pending for examination.

Claims 10 and 13-17 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Taborek, Sr. et al. (U.S. 7,020,729, hereinafter "Taborek)), Grivna (U.S. Patent No. 6,539,051, hereinafter "Grivna"), Wright et al. (U.S. Patent No. 7,103, 049, hereinafter "Wright") in view of Kaufmann (U.S. Patent N. 5,483,539, hereinafter "Kaufmann"). Claims 11-12 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Taborek, Wright, Kaufmann in view of Swoboda et al. (U.S. Patent No. 6,085,336). These obviousness claim rejections are overcome as follows.

Claim 1 has been amended to more clearly define the scope of the invention recited herein. For example, claim 1 is amended to recite, in part, " … a select logic unit for combining a portion of the data word held in the rotator and a portion of data word held in the third register to form a data output block comprising two or more synchronization patterns; a fourth register for storing the data output block; a tester coupled to the fourth register for simultaneously monitoring the two or more synchronization patterns." (Emphasis added)

Support for the amendment to claim 10 is provided, for example, in **Fig. 3**, reproduced in part below for the Examiner's convenience:



> "The output of the variable rotator 308 and the contents of the register 309 are then ***combined*** using selection logic 312 and provided to a register 314, which is 132 bits wide." (Emphasis added, ¶[**0039**])
>
> * * *
>
> "These bit positions are monitored by a sync header test block 310 which determines if they contain proper sync headers. The sync header test block 310 is coupled to a valid frame counter 315 and an invalid frame counter 316. If ***both sync headers are correct***, i.e., if the sync header test block 310 determines that the bits 0, 1 and 66, 67 of register 314 have the proper values (i.e., 0101 or 1010) for a given cycle, the valid frame counter 315 is incremented by two for that cycle." (Emphasis added, ¶[**0041**])

Applicant submits that none of the references cited by the Examiner, taken alone or in combination, teach or suggest each and every element of claim 10 as amended. Claim 10 and its dependent claims 11-17 and 21-23 are thus allowable.

The Examiner acknowledged that Taborek does not disclose at least the first and second registers, the rotator, the selector and many other elements recited in claim 1. (See Office action mailed June 23, 2009, pages 5-6). The Examiner has combined Grivna with Taborek to reject claim 1. Although Grivna appears to disclose the first and second registers and the selector, Grivna, however, fails to teach or suggest the claimed tester coupled to the fourth register for simultaneously monitoring the two or more synchronization patterns, as recited in amended claim 10.

Neither Wright nor Kaufmann appear to teach or suggest at least this claimed element. For example, the portion of Wright cited by the Examiner appears to teach to shift the frame sync signal by one bit time (Wright, col. 2, lines 38-45) to achieve cell delineation, that is, as best understood, Wright appear to teach or suggest that the frame sync position is variable in time and can be shifted to align with the cell boundary instead of searching the frame sync signal in a serialized data stream. Thus, Wright does not teach or suggest the searching of one frame sync pattern let alone simultaneously monitoring two or more synchronization patterns, as recited in claim 10.

While Kaulfmann appears to disclose a state machine and counters for counting valid and invalid frame patterns, Kaufmann fails to teach or suggest the claimed first, second,

third, and fourth registers, the selector, the rotator, the select logic unit, the tester coupled to the fourth register for simultaneously monitoring two or more synchronization patterns, as recited in claim 10.

Claims 11-12 depend from independent claim 10, and are thus patentable over a combination of Taborek, Grivna, Wright, and Kaufmann for at least the same reason as discussed for the allowability of independent claim 10, and more particularly for the specific features they recite. Further, Applicant submits that the deficiencies of Taborek, Grivna, Wright, and Kaufmann are not cured by Swoboda.

Swoboda fails to teach the various features recited in claim 10 discussed above. In fact, Swoboda relates to an electronic processing device and is, therefore, from a different technological field. For example, Swoboda teaches or suggests to independently test an electronic processor (i.e., CPU core) and the on-chip peripheral circuit (i.e., inputs/outputs) by using JTAG boundary scan technique. While Swoboda discloses the term "exhausted" in relation to a "register", this term has a totally different meaning than the claimed exhausted register which keeps track of the bit positions already exhausted by the guesser. The portion of Swoboda cited by the examiner discloses that "the number represented by the contents of shift register 1707 is exhausted" (Swoboda, col. 38, lines 36-39) as a way to set a counter for generating address breakpoint (Swoboda, col. 38, lines 58-62). Thus, Swoboda has no relevance to the present invention, and one of ordinary skill in the art would not have been motivated to use that reference.

Accordingly, Applicants submit that Swoboda, Taborek, Grivna, Wright, and Kaufmann, taken alone or in combination, fail to teach or suggest claims 11 for at least the above reasons. Claim 12 depends from claim 11, and is thus allowable for the same reasons as is claim 11.

New claims 21-25 depend from claim 10, and are thus allowable for at least the same reasons as discussed in claim 10 above. claims 21-25 are supported by the specification as originally filed, so they are not new matter. As explained in the specification (see, e.g., ¶¶[0021], [0041], [0042]), the first and second registers, the selector, the rotator, the guesser, the exhausted register can be 128-bit wide although a 132-bit window would be better suited for a

64b/66b scheme (claim 24), and the first and second counters are reset whenever the system changes states (claim 22).

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

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